

Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) **EP 1 388 878 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
11.02.2004 Bulletin 2004/07

(51) Int Cl.7: **H01J 17/02**

(21) Application number: **03254711.9**

(22) Date of filing: **28.07.2003**

(84) Designated Contracting States:
**AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
HU IE IT LI LU MC NL PT RO SE SI SK TR**
Designated Extension States:
AL LT LV MK

(30) Priority: **06.08.2002 JP 2002228725**

(71) Applicants:
• **FUJITSU LIMITED**
Kawasaki-shi, Kanagawa 211-8588 (JP)
• **Fujitsu Hitachi Plasma Display Limited**
Kawasaki-shi, Kanagawa 213-0012 (JP)

(72) Inventors:
• **Inoue, Kazunori c/o Fujitsu Limited**
Kawasaki-shi Kanagawa 211-8588 (JP)

• **Kasahara, Shigeo c/o Fujitsu Limited**
Kawasaki-shi Kanagawa 211-8588 (JP)
• **Sakita, Koichi c/o Fujitsu Limited**
Kawasaki-shi Kanagawa 211-8588 (JP)
• **Toyoda, Osamu c/o Fujitsu Limited**
Kawasaki-shi Kanagawa 211-8588 (JP)
• **Hasegawa, Minoru c/o Fujitsu Limited**
Kawasaki-shi Kanagawa 211-8588 (JP)
• **Harada, Hideki c/o Fujitsu Limited**
Kawasaki-shi Kanagawa 211-8588 (JP)
• **Betsui, Keiichi c/o Fujitsu Limited**
Kawasaki-shi Kanagawa 211-8588 (JP)

(74) Representative: **Williams, Michael Ian et al**
Haseltine Lake
Imperial House
15-19 Kingsway
London WC2B 6UD (GB)

(54) **Gas discharge panel substrate assembly**

(57) The present invention provides a gas discharge panel substrate assembly comprising: electrodes (3) formed on a substrate, a dielectric layer (4) covering the electrodes (3), and a protective layer (5) covering the

dielectric layer (4) and in contact with a discharge space, wherein the protective layer includes MgO and at least one compound selected from the group consisting of an Al compound, a Ti compound, a Y compound, a Zn compound, a Zr compound, a Ta compound and SiC.

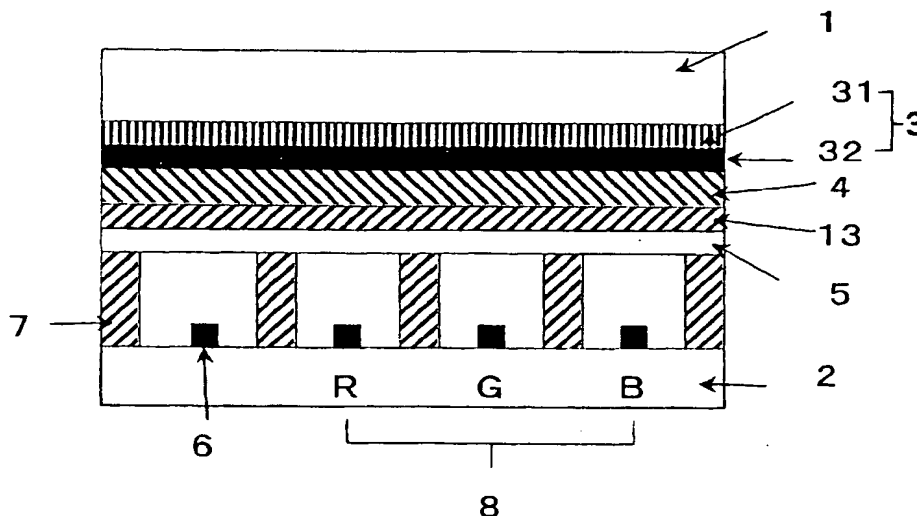


Fig. 4

Description

[0001] The present invention relates to a gas discharge panel substrate assembly, a production method therefore and an AC type gas discharge panel.

[0002] There have been reported on various types of gas discharge panels, among which an AC type plasma display panel (PDP) of a three-electrode surface discharge structure has been introduced to the market.

[0003] Fig. 5 shows a schematic perspective view of a structure of a PDP on the market. The PDP is of a structure in which a front glass substrate 1 and back glass substrate 2 are adhered to each other. Provided on the front glass substrate 1 are display electrodes 3 constituted of transparent electrodes 31 and bus electrodes 32 and the display electrodes 3 are covered with a dielectric layer 4. Further formed on the dielectric layer 4 is a protective layer 5 made of a MgO layer with a high secondary electron emission coefficient. Address electrodes 6 are provided on the back glass substrate 2 so as to intersect with the display electrodes at right angles. Barrier ribs 7 are provided between the address electrodes 6 in order to define light emitting regions and phosphors 8 for red, green and blue are coated on the address electrodes 6 in the respective regions divided by the barrier ribs 7. Ne-Xe gas is sealed in the interior of a space formed by adhering the front glass substrate 1 and the back glass substrate 2 to each other.

[0004] Fig. 6 shows a state of a discharge cell in discharge as viewed in section. A voltage is applied between the display electrodes 3 each including a pair of two electrodes X and Y to form an electric field in a discharge space and to thereby excite Xe and generate gas discharge 9 and vacuum ultraviolet 10 is released therefrom. The ultraviolet 10 strikes the phosphor 8 to emit visible light 11. The discharge cell acts as a display by controlling the vacuum ultraviolet 10 in the electric field in the interior thereof. On this occasion, the vacuum ultraviolet 10 is directed to not only the phosphor 8 but also the front glass substrate 1. The protective layer (MgO layer) 5 and the dielectric layer 4 are formed on the front glass substrate 1 sequentially in the order starting at the discharge surface and since MgO passes a wavelength portion (165 nm or more) of the vacuum ultraviolet therethrough, part of the ultraviolet 10 reaches as far as the dielectric layer 4. In Fig. 6, the reference numbers 2 and 6 are the same as those in Fig. 5 in meaning.

[0005] As a method for forming a dielectric layer for use in a PDP, generally known is a method in which it is formed by dispersing frit glass. The frit glass is provided as a paste obtained by dispersing a glass component into a vehicle made of ethyl cellulose resin as a main component. The frit glass in this form is coated on a substrate by printing and is baked to thereby burn out the resin component with the result of formation of a dielectric layer made of a glass component as a main component. Furthermore, as methods for forming a dielectric layer more suitable for mass production in recent years, there have been proposed: a method in which frit glass in the shape of a sheet obtained by dispersing frit glass in acrylic resin or the like is adhered and baked and a method to use vapor phase film formation such as a CVD method.

[0006] It is desirable to provide a gas discharge panel substrate assembly and a gas discharge panel causing no or little phosphor degradation phenomenon, as well as production methods therefor.

[0007] According to an aspect of the present invention there is provided a gas discharge panel substrate assembly comprising: electrodes formed on a substrate, a dielectric layer covering the electrodes, and a protective layer covering the dielectric layer and in contact with a discharge space, wherein the protective layer includes MgO and at least one compound selected from the group consisting of an Al compound, a Ti compound, a Y compound, a Zn compound, a Zr compound, a Ta compound and SiC.

[0008] Furthermore, another aspect of the present invention provides gas discharge panel substrate assembly comprising: electrodes formed on a substrate, a dielectric layer covering the electrodes, an intermediate layer covering the dielectric layer, and a protective layer covering the intermediate layer and in contact with a discharge space, wherein the protective layer includes MgO and the intermediate layer includes at least one compound selected from the group consisting of an Al compound, a Ti compound, a Y compound, a Zn compound, a Zr compound, a Ta compound and SiC.

[0009] Moreover, according to the present invention, a production method for a gas discharge panel substrate assembly is provided, in which the dielectric layers of the first and second gas discharge panel substrate assemblies are formed with one of a CVD method, a plasma CVD method and a method in which a frit glass in the shape of a sheet is adhered on a substrate, followed by baking.

[0010] Besides, according to the present invention, a production method for a gas discharge panel substrate assembly is provided, in which the intermediate layer of the second gas discharge panel substrate assembly is formed with one of a vacuum evaporation method, a CVD method, a plasma CVD method, a sol-gel method and a binder method.

[0011] Furthermore, according to the present invention, a production method for a gas discharge panel substrate assembly is provided, in which the intermediate layer and the dielectric layer of the second gas discharge panel substrate assembly are continuously formed with a CVD method or a plasma CVD method.

[0012] Moreover, according to the present invention, a production method for a gas discharge panel substrate assembly is provided, in which the intermediate layer and the protective layer of the second gas discharge panel substrate assembly are continuously formed with a vacuum evaporation method.

[0013] Besides, according to the present invention, an AC type gas discharge panel is provided that uses the first

or second gas discharge panel substrate assembly as a gas discharge panel substrate assembly in the front side.

[0014] These and other objects of the present application will become more readily apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the scope of the invention will become apparent to those skilled in the art from this detailed description.

Fig. 1(a) to 1(d) are schematic sectional views showing process steps from formation of the gas discharge panel substrate assembly of the present invention;

Figs. 2(a) to 2(e) are schematic sectional views showing process steps from formation of the gas discharge panel substrate assembly of the present invention;

Fig. 3 is a schematic sectional view of the gas discharge panel of the present invention;

Fig. 4 is a schematic sectional view of the gas discharge panel of the present invention;

Fig. 5 is a schematic perspective view of a structure of a PDP of prior art;

Fig. 6 is a schematic view of a state of a discharge panel in discharge.

[0015] The inventors of the present invention have studied on a relationship between a method for forming a dielectric layer and a chromaticity of a PDP. As a result, it has been found that anomaly in chromaticity occurs in a case where a dielectric layer is formed with the method using frit glass in the shape of a sheet or the vapor phase film formation method such as a Plasma Enhanced CVD (PECVD) method. To be concrete, dielectric layers were formed in formation conditions shown in Table 1, thereafter a protective layer made of a MgO layer was formed by evaporation to a thickness of 1.0 μm and a PDP was formed in an ordinary process, followed by a display quality test on the PDP.

Table 1

Frit paste	Sheet frit	PECVD-SiO ₂
Printing was performed on a glass substrate, after formation of electrodes, with a paste obtained by adding an ethyl cellulose binder to frit glass and the glass substrate with the print was baked in a conveyor type baking furnace under a heating program of 120 min at 350°C and then 30 min at 600°C to form a dielectric layer of 30 μm in thickness.	A sheet obtained by adding an acrylic binder to frit glass is adhered on a glass substrate after formation of electrodes thereon and the glass substrate with the sheet was baked in a conveyor type baking furnace under a heating program of 240 min at 350°C and then 60 min at 600°C to form a dielectric layer of 30 μm in thickness.	After formation of electrodes the glass substrate, SiO ₂ is formed as a dielectric layer on a glass substrate to a thickness of 5 μm in a parallel plate type PECVD apparatus under conditions of feeding SiH ₄ at a flow rate of 900 sccm, N ₂ O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr.

[0016] White chromacity coordinates of a PDP under the conditions for forming a dielectric layer using the frit paste were (0.300, 0.300) in the CIE standard colorimetric system, while being (0.310, 0.285) in a case where the sheet frit was used and furthermore, the coordinates were also (0.320, 0.280) in a case of the PECVD-SiO₂ as well, the two latter of which display a reddish white color. This anomaly in chromaticity was found to be caused by degradation in green phosphor and a shift in chromaticity coordinates to follow, as a result of a study conducted by the inventors.

[0017] It is inferred that discharge generated during a display test causes gas release from a dielectric layer formed with a sheet frit or PECVD and in turn the gas degrades phosphor.

[0018] A gas source can be inferred to be a material, having a hydrocarbon bond, and remained in the layer without being burned out in the baking since the sheet layer prior to the formation of a dielectric layer obtained by using the sheet frit contains much of an organic component. Likewise, in the PECVD method, the source can be inferred to be a material having bonds of hydrogen with silicon and/or carbon such as SiH₄ gas or Si(OC₂H₅)₄ remaining in the layer as a material not reacted due to incomplete decomposition of a process raw gas. It is thought that the materials as the gas source are decomposed under an influence of ultraviolet generated by discharge to release hydrocarbon or hydrogen gas, and the gases pass through the MgO layer to then come out into a discharge space and degrade phosphor. The gases are activated by discharge so as to have a reducing ability; therefore, the activated gases are thought to reduce the protective layer (MgO). The reduced protective layer is colored and therefore deteriorated in transmittance. As the results, a luminance is thought to be degraded during panel display, causing a shift in chromaticity.

[0019] The present invention has, to be concrete, one of features thereof that a protective layer has an ultraviolet shielding function (a first gas discharge substrate assembly) or alternatively, that an intermediate layer having an ultraviolet shielding function is inserted between a dielectric layer and a protective layer (a second gas discharge sub-

strate assembly). The ultraviolet shielding function means a function capable of shielding ultraviolet having 200 nm or less in wavelength mainly.

[0020] In the first gas discharge panel substrate assembly, the protective layer, covering the dielectric layer, and in contact with a discharge space is made of MgO for protecting the dielectric layer from a discharge electric field and at least one compound selected from the group consisting of an Al compound, a Ti compound, an Y compound, a Zn compound, a Zr compound, a Ta compound and SiC having the ultraviolet shielding function.

[0021] As Al compounds, there are exemplified: alumina, aluminum nitride and others, as Ti compounds, there are exemplified: titania, titanium nitride and others, as Y compounds, there are exemplified: yttrium oxide, yttrium nitride and others, as Zn compounds, there are exemplified: zinc oxide, zinc nitride, zinc sulfide and others, as Zr compounds, there are exemplified: zirconium oxide, zirconium nitride and others and as Ta compounds, there are exemplified: tantalum oxide and others.

[0022] The compound having the ultraviolet shielding function is preferably selected from the group consisting of Al_2O_3 (alumina), AlN, TiO_2 (titania), Y_2O_3 (yttrium oxide), ZnO (zinc oxide), ZrO_2 (zirconium oxide), Ta_2O_5 (tantalum oxide) and SiC. Bandgaps of these compounds described above are shown in the following Table 2.

Table 2

	Bandgaps(eV)
MgO	8
Al_2O_3	7.4
AlN	3.8
TiO_2	3.0
Y_2O_3	2.43
ZnO	3.2
ZnS	3.7
ZrO_2	5.16
Ta_2O_5	4.2
SiC	3

[0023] Compounds having a bandgap of 6.2 eV or less among the compounds described above are preferably used since the compounds exert a vacuum ultraviolet (VUV) shielding effect.

[0024] A mixing ratio of MgO and the compound having the ultraviolet shielding function is different according to a kind of a compound in use and the ratio is preferably in the range of from 95 to 85, to 5 to 15 in wt %. If a percentage of the compound having the ultraviolet shielding function is less than 5 wt %, it is not preferably since the ultraviolet shielding effect is reduced, while if the percentage of the compound is more than 15, it is not preferably either since a secondary electron emission ratio is decreased.

[0025] No specific limitation is imposed on a thickness of the protective layer as far as a prescribed function is exerted, but it is preferably in the range of from 0.5 to 1.5 μm .

[0026] No specific limitation is imposed on a method for forming a protective layer but any of known methods in the technical field pertaining to the present invention can be used. There can be exemplified: a CVD method, a sputter method and a vacuum or an atmospheric evaporation method and among them, the vacuum evaporation method is preferably used.

[0027] The CVD method is a method in which a raw gas (for example, a chloride) of a compound from which a protective layer is made is heated and decomposed to deposit a desired compound onto a substrate.

[0028] The sputter method is a method in which a compound from which a protective layer is made is sputtered by an inert gas to deposit a desired compound onto a substrate.

[0029] The evaporation method is a method in which a compound from which a protective layer is made is evaporated by heating with heating means such as an electron beam or the like to deposit a desired compound onto a substrate.

[0030] On the other hand, in the second gas discharge panel substrate assembly, the intermediate layer located between the dielectric layer and the protective layer is made of at least one compound selected from the group consisting of an Al compound, a Ti compound, an Y compound, a Zn compound, a Zr compound, a Ta compound and SiC, all having the ultraviolet shielding function. As concrete examples of the compounds, there are shown the same compounds as for the first gas discharge panel substrate assembly. Furthermore, similar to the first discharge panel substrate assembly, preferable are compounds having 6.2 eV or less in bandgap.

[0031] No specific limitation is imposed on a thickness of the intermediate layer as far as a prescribed function is exerted but it is preferably in the range of from 0.1 to 1 μm .

[0032] As methods for forming the intermediate layer, there are exemplified: a vacuum evaporation method, a CVD method, a plasma CVD method, a sol-gel method, a binder method and others.

[0033] The vacuum evaporation method is a method in which a compound from which an intermediate layer is made is heated and evaporated under a vacuum of 10^{-3} to 10^{-8} Torr with heating means such as an electron beam to deposit a desired compound onto a substrate.

[0034] The CVD method is a method in which a raw gas (for example, a chloride) of a compound from which an intermediate layer is made is heated and decomposed by heating to deposit a desired compound onto a substrate.

[0035] The plasma CVD method is a method in which a raw gas (for example, a chloride) of a compound from which an intermediate layer is made is decomposed with a plasma to deposit a desired compound onto a substrate.

[0036] The sol-gel method is a method in which a solution containing a fatty acid salt or an alkoxide of a compound from which an intermediate layer is made is coated on a substrate to bake a coat on the substrate and to thereby form the intermediate layer.

[0037] The binder method is a method in which a solution or a dispersion containing a compound from which an intermediate layer is made is coated on a substrate to bake a coat on the substrate and to thereby form the intermediate layer.

[0038] Note that in the second gas discharge panel substrate assembly, the protective layer, formed on the intermediate layer, and in contact with the discharge space is preferably made of MgO and a thickness thereof is preferably in the range of from 0.5 to 1.5 μm . Methods for forming the protective layer can be methods similar to the methods for use in the first gas discharge panel substrate assembly.

[0039] By imparting the protective layer the ultraviolet shielding function, the number of production steps can be decreased compared with a construction in which the intermediate layer has an ultraviolet shielding function and as a result, a tact is improved and a cost is reduced.

[0040] Structural members of the first and second gas discharge panel substrate assemblies other than the protective layer and the intermediate layer can be the same as each other.

[0041] No specific limitation is imposed on a substrate, but any of known substrates in the technical field pertaining to the present invention can be used. To be concrete, there are exemplified: transparent substrates such as a glass substrate and a plastic substrate.

[0042] No specific limitation is imposed on an electrode formed on a substrate, but any of known electrodes in the technical field pertaining to the present invention can be used. To be concrete, there are exemplified transparent electrodes such as ITO and NESA. Furthermore, a metal electrode made of Cr, Cu or a stacked structure thereof may be formed on a transparent electrode in order to reduce a resistance of the transparent electrode. An arrangement of electrodes are formulated ordinarily in an array of stripes on a substrate, though being different according to a kind of a gas discharge panel.

[0043] As the dielectric layer covering electrodes, no specific limitation is imposed on a dielectric layer but any of known dielectric in the technical field pertaining to the present invention can be used. To be concrete, there are exemplified: layers made of a low-melting glass and SiO_2 .

[0044] The low-melting glass exemplified in the first place can be formed using a frit paste or a sheet frit. The frit paste can be obtained by adding an ethyl cellulose binder and a solvent (arbitrary) to a low-melting glass (frit glass). The frit paste is coated at a prescribed position with a printing method or the like to bake the coat and to thereby obtain the dielectric layer. A sheet frit can be obtained by adding an acrylic binder to frit glass to form a mixture in the shape of a sheet. The sheet frit is adhered onto a substrate and then the sheet is baked to thereby transform the sheet into the dielectric layer. The dielectric layer made of a low-melting glass ordinarily has a thickness in the range of from 15 to 35 μm .

[0045] SiO_2 , which is exemplified in the second place, can be formed with a CVD method or a PECVD method. To be concrete, the SiO_2 dielectric layer can be formed such that, in a case of the PECVD method, a parallel plate type plasma CVD apparatus can be used to decompose a silane gas such as SiH_4 or Si_2H_6 or a silicon containing compound such as tetraorthoethyl silicate (TEOS) with a plasma generated under conditions of an RF output in the range of from 1 to 2 kW, a temperature in the range of from 300 to 400°C and a pressure in the range of 1 to 3 Torr. The SiO_2 dielectric layer also may be formed with an atmospheric CVD method. The dielectric layer made of SiO_2 ordinarily has a thickness in the range of from 5 to 15 μm .

[0046] Among the methods for forming the dielectric layer, preferable are a method forming a dielectric layer using a sheet frit and vapor phase methods such as a CVD method and a PECVD method because of the following reason and easiness in production.

[0047] In the dielectric layer formed with a sheet frit among the dielectric layers described above, since much of an organic component is contained in a sheet layer prior to the formation, it is inferred that a material having a hydrocarbon bond remains in the layer without burning out in baking. Furthermore, it is thought that in the vapor phase method, a

material having bonds of silicon and/or carbon with hydrogen such as SiH_4 or $\text{Si}(\text{OC}_2\text{H}_5)_4$ is not all decomposed and partly remains unreacted in the formed film. It is thought that the material is decomposed by ultraviolet generated by discharge to release hydrocarbon or hydrogen gas, and the gas passes through a MgO layer and is released into a discharge space to degrade a phosphor. Furthermore, it is thought that since the gas is activated by discharge so as to have a reducing ability, the protective layer (MgO layer) is also reduced. The reduced protective layer is colored to degrade a transmittance. It is thought that with such results, a luminance is degraded during panel display to alter chromaticity. In the present invention, the ultraviolet shielding function is imparted to the protective layer of the first gas discharge panel substrate assembly and the intermediate layer of the second gas discharge panel substrate assembly. Therefore, it is prevented from occurring that ultraviolet generated in the discharge space reaches a dielectric layer, thereby enabling generation of hydrocarbon or hydrogen to be prevented.

[0048] Note that since even in a case where a frit paste is used as well, it is thought that a material having a hydrocarbon bond exists in the dielectric layer, a construction of the present invention is useful.

[0049] In formation of the protective layer, and intermediate layer and dielectric layer, all described above, the intermediate layer and the dielectric layer may be formed continuously with a CVD method or a plasma CVD method, and the intermediate layer and the protective layer may be formed continuously with a vacuum evaporation method. By forming continuously, reduction in production time can be achieved and mixing into of an impurity to layers can be prevented.

[0050] Description will be given of an example of a production method for a first gas discharge panel substrate assembly of the present invention below with reference to Figs. 1(a) to 1(d). Figs. 1(a) to 1(d) are schematic sectional views showing process steps from formation of the display electrodes (transparent electrodes and bus electrodes) to formation of a protective layer in the substrate side.

[0051] Transparent electrodes 31 are at first formed on a glass substrate (Fig. 1(a)), subsequent to this bus electrodes (for example, a three layer structure of Cr/Cu/Cr) 32 are formed (Fig. 1(b)) and display electrodes (also referred to as sustaining electrodes) 3 are thereby formed. The transparent electrodes and the bus electrodes can be formed with a known method.

[0052] Then, a dielectric layer 4 covering display electrodes 3 is formed (Fig. 1(c)). As methods for forming the dielectric layer 4, there are available a method in which a frit paste containing a frit glass or a sheet frit is used and a vapor phase method such as a CVD method.

[0053] A protective layer 12 having the ultraviolet shielding function is formed at a final stage (Fig. 1(d)). As methods for forming the protective layer 12, there can be used vapor phase film formation methods such as a CVD method, a vacuum or atmospheric evaporation method and a sputter method.

[0054] Then, description will be given of an example of a production method for a second gas discharge panel substrate assembly of the present invention below with reference to Figs. 2(a) to 2(e). Figs. 2(a) to 2(e) are schematic sectional views showing process steps from formation of display electrodes (a transparent electrodes and bus electrodes) to formation of a protective layer in the substrate side.

[0055] Transparent electrodes 31 are at first formed on a glass substrate (Fig. 2(a)), subsequent to this bus electrodes 32 are formed (Fig. 2(b)) and display electrodes (also referred to as sustaining electrodes) 3 are thereby formed. The transparent electrodes and bus electrodes can be formed with a known method.

[0056] Then, a dielectric layer 4 covering the display electrodes 3 is formed (Fig. 2(c)). As methods for forming the dielectric layer 4, there are available a method in which a frit paste containing a frit glass or a sheet frit is used and a vapor phase method such as a CVD method.

[0057] Then, an intermediate layer 13 having the ultraviolet shielding function is formed (Fig. 2(d)). As a method for forming the intermediate layer 13, there can be used: a vacuum evaporation method, a CVD method, a sol-gel method, or a binder method.

[0058] A protective layer 5 is formed at a final stage (Fig. 2(e)). As methods for forming the protective layer 5, there are generally exemplified: vapor phase methods such as an evaporation method, a sputter method and others.

[0059] Then, description will be given of a structure of a gas discharge panel (PDP) in a case where a gas discharge panel substrate assembly of the present invention is used in the front side below with reference to Figs. 3 and 4.

[0060] PDPs of Figs. 3 and 4 are three-electrode AC type surface discharge PDPs. The PDPs illustrate cases where, in each case, sub-pixels (discharge cells) are formed with barrier ribs arranged in an array of stripes. The PDP of Fig. 3 is a PDP in which the first gas discharge panel substrate assembly is used and the PDP of Fig. 4 is a PDP in which the second gas discharge panel substrate assembly is used.

[0061] The PDP of Fig. 3 is constituted of a front substrate and a back substrate.

[0062] The first gas discharge panel substrate assembly obtained in the process of Fig. 1 is used as the front substrate as it is.

[0063] Then, the back substrate is generally constituted of: plural address electrodes 6 each in the shape of a stripe formed on a back glass substrate 2; plural barrier ribs 7 each in the shape of a stripe formed on the back glass substrate 2 between the adjacent address electrodes 6; and phosphors 8 formed between the barrier ribs 7 and on rib surfaces

thereof. In Fig. 3, the phosphors 8 include: phosphors for red (R), green (G) and blue (B).

[0064] Furthermore, the dielectric layer is formed on the back glass substrate 2 so as to cover the address electrodes 6 and the barrier ribs 7 may be formed on the dielectric layer. The dielectric layer can be formed in a similar way to that adopted in forming the dielectric layer in the front substrate side.

[0065] The PDP of Fig. 4 has one of features that an ultraviolet shielding function is not imparted to the protective layer, as in the PDP of Fig. 3, but the intermediate layer having an ultraviolet shielding function is formed between the protective layer and the dielectric layer. The PDP of Fig. 4 is the same as the PDP of Fig. 3 with the exception of this particular structure.

EXAMPLES

[0066] While description will be given of the present invention below with examples and comparative examples in a further concrete manner, no limitation is placed on conditions for forming a film, thickness values of films, materials and others used therein.

Example 1 (a dielectric layer constituted of a PECVD-SiO₂ and a protective layer having an ultraviolet shielding function constituted of simultaneous electron beam evaporation-MgO, and-ZrO₂, alumina, titania, Y₂O₃, ZnS, Ta₂O₅ or SiC)

[0067] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Then, ZrO₂ and MgO were simultaneously deposited by electron beam evaporation to obtain a protective layer of a thickness of 1.0 μm. Thereafter, a PDP with the following specifications was fabricated by an ordinary process, followed by a display quality test on the PDP.

(Specifications of the PDP)

[0068]

a screen size: 42 inch
 the number of pixels: 852 x 480 (VGA)
 the number of sub-pixels: 2556 x 480
 a sub-pixel size: 1080 μm x 390 μm
 material of front substrate: soda lime glass
 thickness of front substrate: 3 mm
 width of transparent electrode: 275 μm
 width of bus electrode: 100 μm
 surface discharge gap: 100 μm
 width of light shielding layer between transparent electrodes: 350 μm
 width of barrier rib: 70 μm
 height of barrier rib: 140 μm
 barrier rib pitch: 360 μm
 kinds of phosphors: PDP standard RGB phosphors, red (Y, Gd)BO₃:Eu, green Zn₂SiO₄:Mn, blue BaMgAl₁₀O₁₇:Eu
 driving conditions: 25 kHz at 180 V

(Display Quality Test)

[0069] White display at a load ratio of 10 % is measured with a luminance meter BM7 made by TOPCON CORPORATION.

[0070] As a result of the test, chromaticity coordinates in the CIE standard colorimetric system were (0.300, 0.301) and anomaly in chromaticity was suppressed.

[0071] Furthermore, PDPs were fabricated in specifications and conditions similar to those described above with the exception that ZrO₂ was substituted for alumina, titania, Y₂O₃, ZnS, Ta₂O₅ or SiC. Coordinates of chromaticity of obtained PDPs are (0.301, 0.298), (0.301, 0.298), (0.303, 0.298), (0.302, 0.298), (0.300, 0.300) and (0.302, 0.298), which showed that degradation was suppressed.

Example 2 (a dielectric layer constituted of a PECVD-SiO₂ and an intermediate layer constituted of electron beam evaporation-ZrO₂, alumina, titania, Y₂O₃, ZnS, Ta₂O₅ or SiC)

[0072] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Then, an intermediate layer made of ZrO₂ was deposited by electron beam evaporation to a thickness of 0.3 μm. Subsequent to this a protective layer made of MgO is evaporation deposited to a thickness of 1.0 μm. Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.302), which showed that anomaly in chromaticity was suppressed.

[0073] Furthermore, PDPs were fabricated in specifications and conditions similar to those described above with the exception that intermediate layers were made of alumina, titania, Y₂O₃, ZnS, Ta₂O₅ and SiC respectively. Chromaticity coordinates were (0.302, 0.299), (0.302, 0.299), (0.301, 0.298), (0.301, 0.299), (0.300, 0.300) and (0.301, 0.299), which showed that degradation was suppressed.

Example 3 (a dielectric layer constituted of a PECVD-SiO₂ and an intermediate layer constituted of a binder method titania-TiO₂)

[0074] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Then, titania powder of 0.5 μm in average particle diameter was dispersed in a binder composed of 5 wt % ethylcellulose and 95 wt % terpineol, a coat was applied on the dielectric layer by a printing method, thereafter the coat was baked in the atmosphere at 400°C for 30 min to form an intermediate layer made of TiO₂ with a thickness of 3.0 μm. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm. Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.299), which showed that anomaly in chromaticity was suppressed.

Example 4 (a dielectric layer constituted of a PECVD-SiO₂ and an intermediate layer constituted of a sol-gel method titania-TiO₂)

[0075] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Then, Ti(OC₂H₅)₄ and 0.5 % dilute hydrochloric acid were mixed in a molar ratio of 1 to 8, a reaction was performed therebetween for 30 min, thereafter the mixture was diluted with ethanol to a volume ten times the original, the diluted mixture was coated on the dielectric layer with a spin coat method to form a coat, thereafter the coat was baked in the atmosphere at 400°C for 30 min to thereby form an intermediate layer made of TiO₂ of 3.0 μm in thickness. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm. Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.300, 0.299), which showed that anomaly in chromaticity was suppressed.

Example 5 (a dielectric layer constituted of a PECVD-SiO₂ and an intermediate layer constituted of an atmospheric CVD titania of isopropyl titanate-TiO₂)

[0076] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Then, in an atmospheric CVD apparatus, an intermediate layer made of TiO₂ of 1.0 μm in thickness was formed under conditions of Ti[COH(CH₃)₂]₄ at a flow rate of 100 sccm, O₂ at a flow rate of 500 sccm and a substrate temperature at 400°C. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm. Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.298), which showed that anomaly in chromaticity was suppressed.

Example 6 (a dielectric layer constituted of a PECVD-SiO₂ and an intermediate layer constituted of an atmospheric CVD, titania of titanium tetrachloride-TiO₂)

[0077] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Then, in an atmospheric CVD apparatus, an intermediate layer made of TiO₂ of 0.3 μm in thickness was formed under conditions of TiCl₄ at a flow rate of 100 sccm, O₂ at a flow rate of 500 sccm and a substrate temperature at 400°C. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm. Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.298), which showed that anomaly in chromaticity was suppressed.

Example 7 (a dielectric layer constituted of a PECVD-SiO₂ and an intermediate layer constituted of an atmospheric CVD of zirconium tetrachloride-ZrO₂)

[0078] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Then, in an atmospheric CVD apparatus, an intermediate layer made of ZrO₂ of 0.3 μm in thickness was formed under conditions of ZrCl₄ at a flow rate of 100 sccm, O₂ at a flow rate of 500 sccm and a substrate temperature at 480°C. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm. Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.299), which showed that anomaly in chromaticity was suppressed.

Example 8 (a dielectric layer constituted of a PECVD-SiO₂ and an intermediate layer constituted of a plasma CVD alumina-Al₂O₃)

[0079] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr and successively, in the same apparatus, an intermediate layer made of Al₂O₃ of 0.3 μm in thickness was formed under conditions of AlCl₃ at a flow rate of 100 sccm, CO₂ at a flow rate of 1000 sccm, H₂ at flow rate of 500 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm. Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.300), which showed that anomaly in chromaticity was suppressed.

Example 9 (a dielectric layer constituted of a sheet frit-low-melting glass and an intermediate layer constituted of an electron beam evaporation-ZrO₂)

[0080] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter an acrylic binder was added to frit glass made of PbO-B₂O₅-SiO₂ to process the mixture into a sheet, the sheet was adhered onto the substrate and baked in a conveyor type baking furnace under a heating program of 240 min at 350°C and thereafter 60 min at 600°C, thereby forming an dielectric layer of 30 μm in thickness. Then, an intermediate layer made of ZrO₂ was formed with electron beam evaporation to a thickness of 0.3 μm. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm. Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.299), which showed that anomaly in chromaticity was suppressed.

Example 10 (a dielectric layer constituted of a PECVD-SiO₂ and an intermediate layer constituted of an electron beam evaporation-ZrO₂)

[0081] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under con-

ditions of TEOS at a flow rate of 800 sccm, O₂ at a flow rate of 2000 sccm, an RF output at 1.5 kW, a temperature at 350°C and a pressure at 1.0 Torr. Note that dielectric layers formed on a silicon substrate and a soda lime substrate had stresses of 0.7E9 dyn/cm² and -1.9 dyn/cm², respectively. Thereafter an intermediate layer made of ZrO₂ was deposited to a thickness of 0.3 μm by electron beam evaporation. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm.

[0082] Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.299), which showed that anomaly in chromaticity was suppressed.

Example 11 (a dielectric layer constituted of a CVD-SiO₂ and an intermediate layer constituted of an electron beam evaporation-ZrO₂)

[0083] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in an atmospheric CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 1000 sccm, N₂O at a flow rate of 10000 sccm, and a temperature at 450°C. Note that dielectric layers formed on a silicon substrate and a soda lime substrate had stresses of +4E9 dyn/cm² and +2.3 dyn/cm², respectively. Thereafter an intermediate layer made of ZrO₂ was deposited to a thickness of 0.3 μm by electron beam evaporation. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm.

[0084] Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.301, 0.299), which showed that anomaly in chromaticity was suppressed.

Example 12 (a dielectric layer constituted of a CVD-SiO₂ and an intermediate layer constituted of a plasma CVD tantalum oxide-Ta₂O₅)

[0085] Transparent electrodes and bus electrodes were formed on a substrate in the front side, thereafter in a parallel plate type plasma CVD apparatus, a dielectric layer made of SiO₂ was formed to a film thickness of 5 μm under conditions of SiH₄ at a flow rate of 900 sccm, N₂O at a flow rate of 9000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 3.0 Torr. Successively, in the same apparatus, an intermediate layer made of Ta₂O₅ of 0.2 μm in thickness was formed under conditions of Ta(C₂H₅OH)₅ at a flow rate of 200 sccm (supplied directly after evaporation), O₂ at a flow rate of 1000 sccm, an RF output at 2.0 kW, a temperature at 400°C and a pressure at 4.0 Torr. Subsequent to this a protective layer made of MgO layer was deposited by evaporation to a thickness of 1.0 μm.

[0086] Thereafter, a PDP was fabricated in specifications and conditions similar to those adopted in Example 1, followed by a display quality test on the PDP. As a result of the test, chromaticity coordinates were (0.300, 0.300), which showed that anomaly in chromaticity was suppressed.

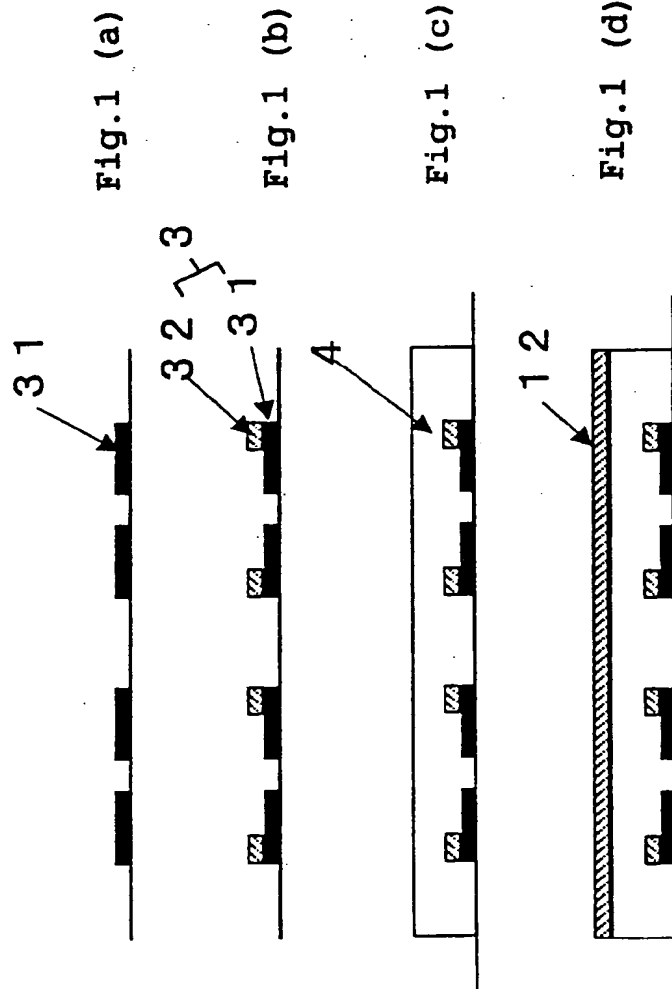
[0087] Note that, in the present invention, no specific limitation is imposed on the examples described above, but various modification or alterations can be included. For example, a structure can also be included in which a substrate provided with a dielectric layer, barrier ribs and phosphor layers thereon is arranged in the front side and a substrate provided with a protective layer and others thereon is arranged in the back side. Another structure can also be included in which address electrodes are covered with a dielectric layer, and barrier ribs and phosphor layers are formed on the dielectric layer, in which case a surface of the dielectric layer is desirably covered with an ultraviolet shielding film. Furthermore, the present invention can also be applied to two-electrode AC type opposite discharge PDP.

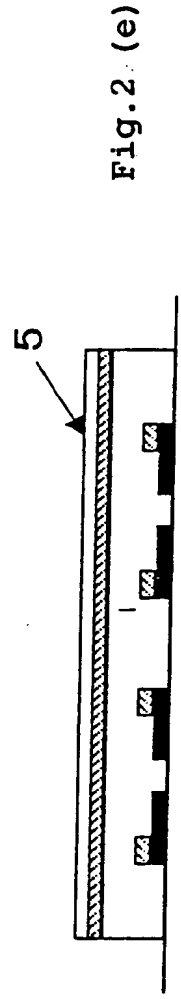
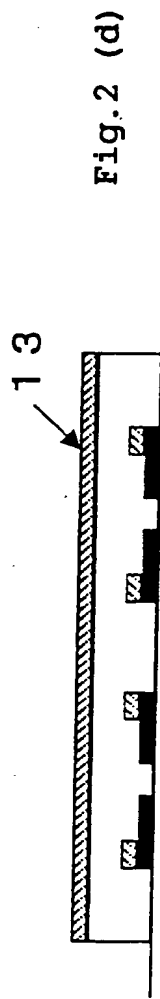
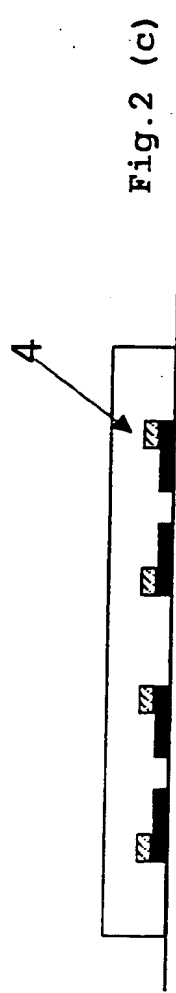
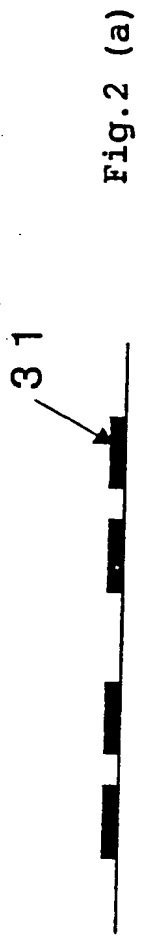
[0088] According to the present invention, by imparting a protective layer itself an ultraviolet shielding function or inserting an intermediate layer having an ultraviolet shielding function between a protective layer and a dielectric layer, vacuum ultraviolet generated during discharge is prevented from reaching the dielectric layer, thereby disabling disconnection of a hydrocarbon bond in the dielectric layer. Therefore, since suppression can be realized of reduction of phosphor and the protective layer caused by hydrogen generated by the disconnection, there can be obtained a gas discharge panel without degradation of phosphor.

Claims

1. A gas discharge panel substrate assembly comprising: electrodes formed on a substrate, a dielectric layer covering the electrodes, and a protective layer covering the dielectric layer and in contact with a discharge space, wherein the protective layer includes MgO and at least one compound selected from the group consisting of an Al compound, a Ti compound, a Y compound, a Zn compound, a Zr compound, a Ta compound and SiC.

2. A gas discharge panel substrate assembly of claim 1, wherein the protective layer comprises a layer which does not transmit light having a wavelength of 200 nm or less.
- 5 3. A gas discharge panel substrate assembly of claim 1 or 2, wherein said at least one compound selected from the group consisting of an Al compound, a Ti compound, a Y compound, a Zn compound, a Zr compound, a Ta compound and SiC is a compound having a bandgap of 6.2 eV or less.
- 10 4. A gas discharge panel substrate assembly of claim 1, 2 or 3, wherein the dielectric layer contains a low-melting glass or CVD-SiO₂.
- 15 5. A gas discharge panel substrate assembly comprising: electrodes formed on a substrate, a dielectric layer covering the electrodes, an intermediate layer covering the dielectric layer, and a protective layer covering the intermediate layer and in contact with a discharge space, wherein the protective layer includes MgO and the intermediate layer includes at least one compound selected from the group consisting of an Al compound, a Ti compound, a Y compound, a Zn compound, a Zr compound, a Ta compound and SiC.
- 20 6. A gas discharge panel substrate assembly of claim 5, wherein said at least one compound selected from the group consisting of an Al compound, a Ti compound, a Y compound, a Zn compound, a Zr compound, a Ta compound and SiC is a compound having a bandgap of 6.2 eV or less.
- 25 7. A gas discharge panel substrate assembly of claim 5 or 6, wherein the intermediate layer comprises a layer which does not transmit light having a wavelength of 200 nm or less.
- 30 8. A gas discharge panel substrate assembly of claim 5, 6 or 7, wherein the dielectric layer contains a low-melting glass or CVD-SiO₂.
- 35 9. A production method for a gas discharge panel substrate assembly, wherein the dielectric layer as claimed in claim 1, 2, 3 or 4 is formed with one of a CVD method, a plasma CVD method and a method in which a frit glass in the shape of a sheet is adhered on a substrate, followed by baking.
- 40 10. A production method for a gas discharge panel substrate assembly, wherein the dielectric layer as claimed in claim 5, 6, 7 or 8 is formed with one of a CVD method, a plasma CVD method and a method in which a frit glass in the shape of a sheet is adhered on a substrate, followed by baking.
- 45 11. A production method for a gas discharge panel substrate assembly, wherein the intermediate layer as claimed in claim 5, 6, 7 or 8 is formed with one of a vacuum evaporation method, a CVD method, a plasma CVD method, a sol-gel method and a binder method.
- 50 12. A production method for a gas discharge panel substrate assembly, wherein the intermediate layer and the dielectric layer as claimed in claim 5, 6, 7 or 8 are continuously formed with a CVD method or a plasma CVD method.
- 55 13. A production method for a gas discharge panel substrate assembly, wherein the intermediate layer and the protective layer as claimed in claim 5, 6, 7 or 8 are continuously formed with a vacuum evaporation method.
14. An AC type gas discharge panel using the gas discharge panel substrate assembly as claimed in claim 1, 2, 3 or 4 as a gas discharge panel substrate assembly in the front side.
15. An AC type gas discharge panel using the gas discharge panel substrate assembly as claimed in claim 5, 6, 7 or 8 as a gas discharge panel substrate assembly in the front side.





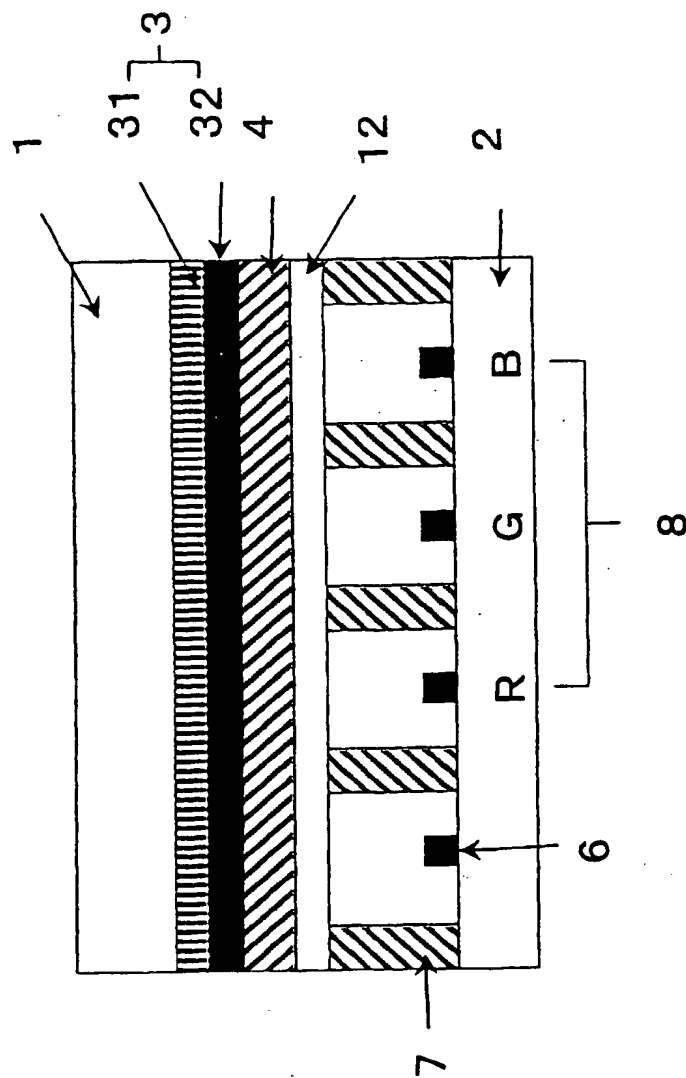


Fig.3

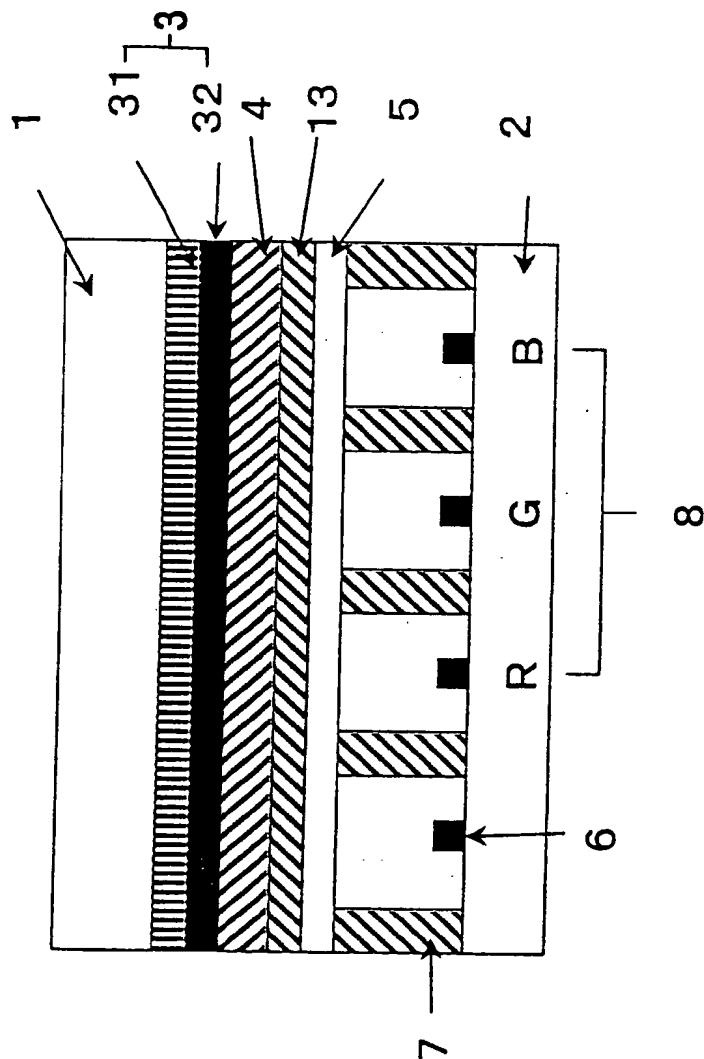


Fig. 4

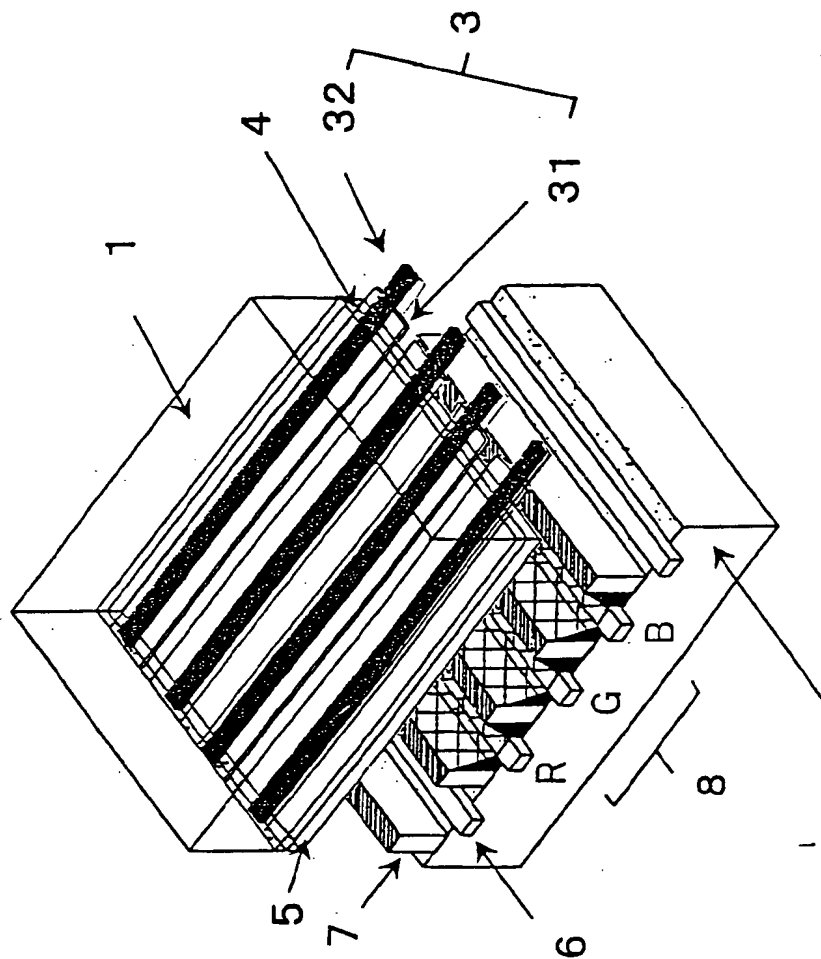


Fig. 5

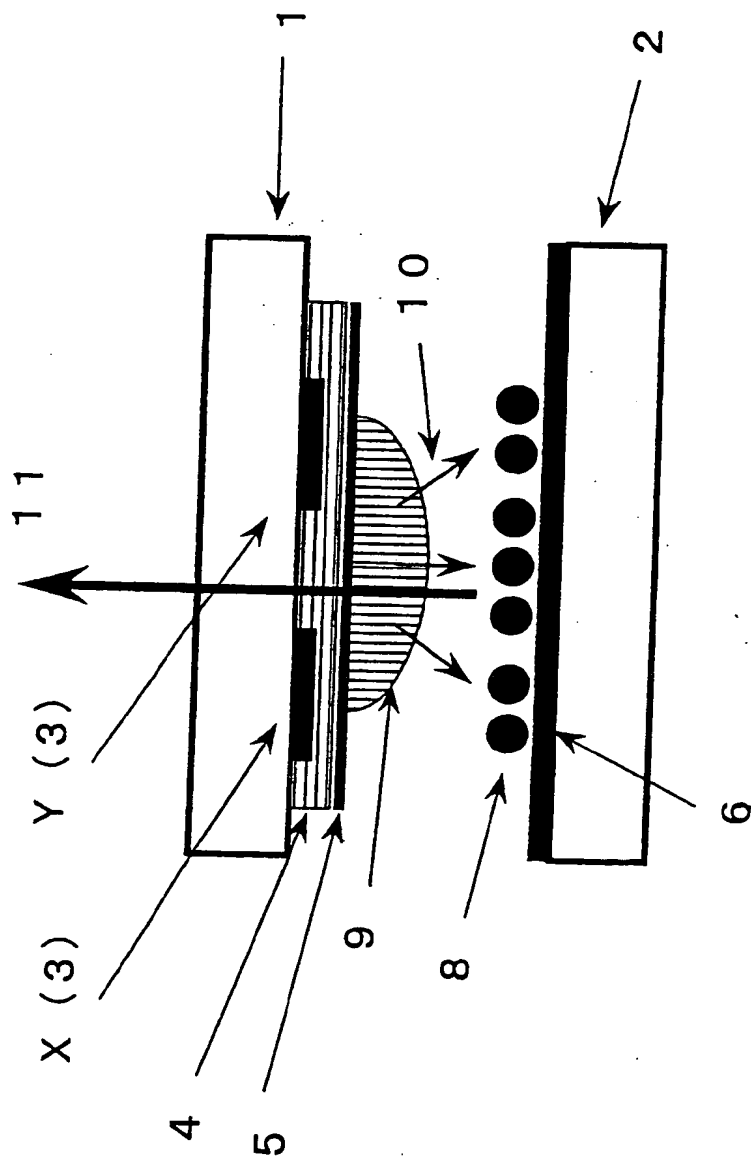


Fig. 6



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 25 4711

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 454 861 A (HASEGAWA HIROMI ET AL) 3 October 1995 (1995-10-03) abstract * column 3, line 21-30; figure 1 * * column 8, line 11-21 *	1	H01J17/02
X	EP 0 881 657 A (FUJITSU LTD) 2 December 1998 (1998-12-02) * page 4, line 11-16; figure 4 * * page 4, column 32-36 *	1	
P,X	EP 1 237 175 A (HITACHI LTD) 4 September 2002 (2002-09-04) abstract * figure 1 *	1	
A	EP 1 221 708 A (MATSUSHITA ELECTRIC IND CO LTD) 10 July 2002 (2002-07-10)		
A	EP 1 085 554 A (PHILIPS CORP INTELLECTUAL PTY ; KONINKL PHILIPS ELECTRONICS NV (NL)) 21 March 2001 (2001-03-21) abstract * figure 1 *	2	
P,X	EP 1 258 902 A (PHILIPS CORP INTELLECTUAL PTY ; KONINKL PHILIPS ELECTRONICS NV (NL)) 20 November 2002 (2002-11-20) * paragraphs [0018], [0024]-[0027], [0029]-[0031]; figure 3 *	5	
A	US 2001/022498 A1 (YOO MIN-SUN) 20 September 2001 (2001-09-20) * paragraphs [0035], [0036]; figures 3,4 *	5	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01J
The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 14 November 2003	Examiner Centmayer, F
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1500-03-02 (P04001)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 03 25 4711

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

14-11-2003

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 5454861	A	03-10-1995	JP	3282882 B2	20-05-2002
			JP	6316671 A	15-11-1994
EP 0881657	A	02-12-1998	JP	3247632 B2	21-01-2002
			JP	10334809 A	18-12-1998
			DE	69723676 D1	28-08-2003
			EP	1300869 A1	09-04-2003
			EP	0881657 A2	02-12-1998
			US	6242864 B1	05-06-2001
EP 1237175	A	04-09-2002	JP	2002260535 A	13-09-2002
			EP	1237175 A2	04-09-2002
			US	2002121861 A1	05-09-2002
EP 1221708	A	10-07-2002	EP	1221708 A2	10-07-2002
			EP	1221709 A2	10-07-2002
			EP	1221711 A2	10-07-2002
			EP	1164620 A2	19-12-2001
			EP	1333462 A2	06-08-2003
			DE	69630004 D1	23-10-2003
			EP	0779643 A2	18-06-1997
			JP	3339554 B2	28-10-2002
			JP	10125237 A	15-05-1998
			JP	2002093327 A	29-03-2002
			US	5770921 A	23-06-1998
			US	5993543 A	30-11-1999
EP 1085554	A	21-03-2001	DE	19944202 A1	22-03-2001
			EP	1085554 A1	21-03-2001
			JP	2001118511 A	27-04-2001
			TW	472274 B	11-01-2002
EP 1258902	A	20-11-2002	DE	10122287 A1	14-11-2002
			CN	1389893 A	08-01-2003
			EP	1258902 A2	20-11-2002
			JP	2002358893 A	13-12-2002
			US	2003038598 A1	27-02-2003
US 2001022498	A1	20-09-2001	KR	247821 B1	15-03-2000
			CN	1210323 A	10-03-1999
			FR	2767962 A1	05-03-1999
			JP	11120924 A	30-04-1999

EPOFORM/1455

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82